



#11/Drawing  
4413  
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED

In re application of

Docket No: Q55026

APR 03 2003

Tetsuya AKIMOTO, et al.

Technology Center 2100

Appln. No.: 09/347,409

Group Art Unit: 2123

Confirmation No.: 3821

Examiner: DAY, HERNG-DER

Filed: July 6, 1999

For: METHOD AND COMPUTER SOFTWARE PRODUCT FOR CALCULATING AND  
PRESENTING A NUMERICAL VALUE REPRESENTATIVE OF A PROPERTY OF  
A CIRCUIT (As Amended)

### SUBMISSION OF DRAWINGS

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Submitted herewith please find four (4) sheets of drawings in compliance with  
37 C.F.R. § 1.84. The Examiner is respectfully requested to acknowledge receipt of these  
drawings.

The submitted drawings incorporate the proposed drawing changes approved in Paper  
No. 8 and are believed to obviate the informalities indicated on Form PTO-948 attached to Paper  
No. 5.

Respectfully submitted,

George Brieger  
Registration No. P-52,652

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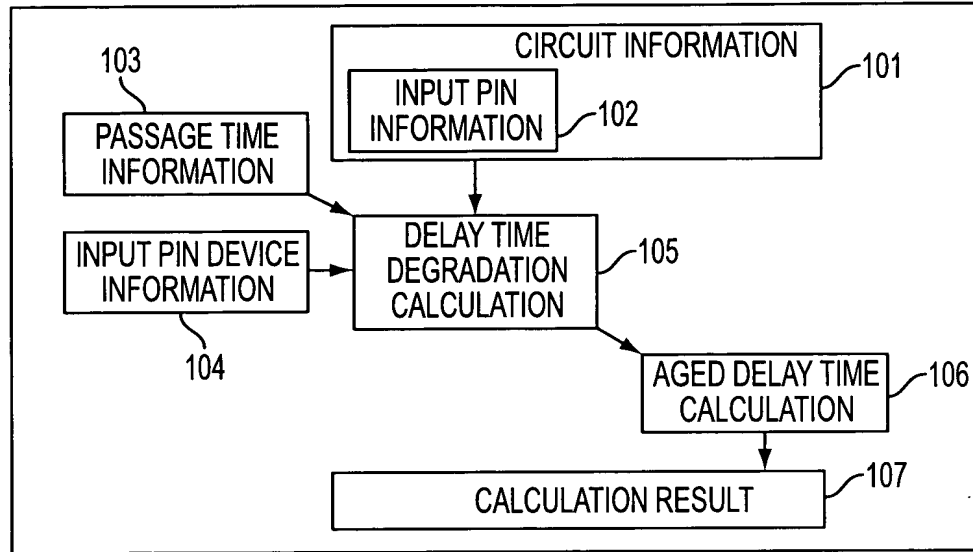
WASHINGTON OFFICE



23373

PATENT TRADEMARK OFFICE

Date: April 1, 2003



A CONVENTIONAL METHOD OF  
CALCULATING AGED DELAY TIME  
OF A LOGIC LEVEL CIRCUIT

FIG. 1  
(PRIOR ART)

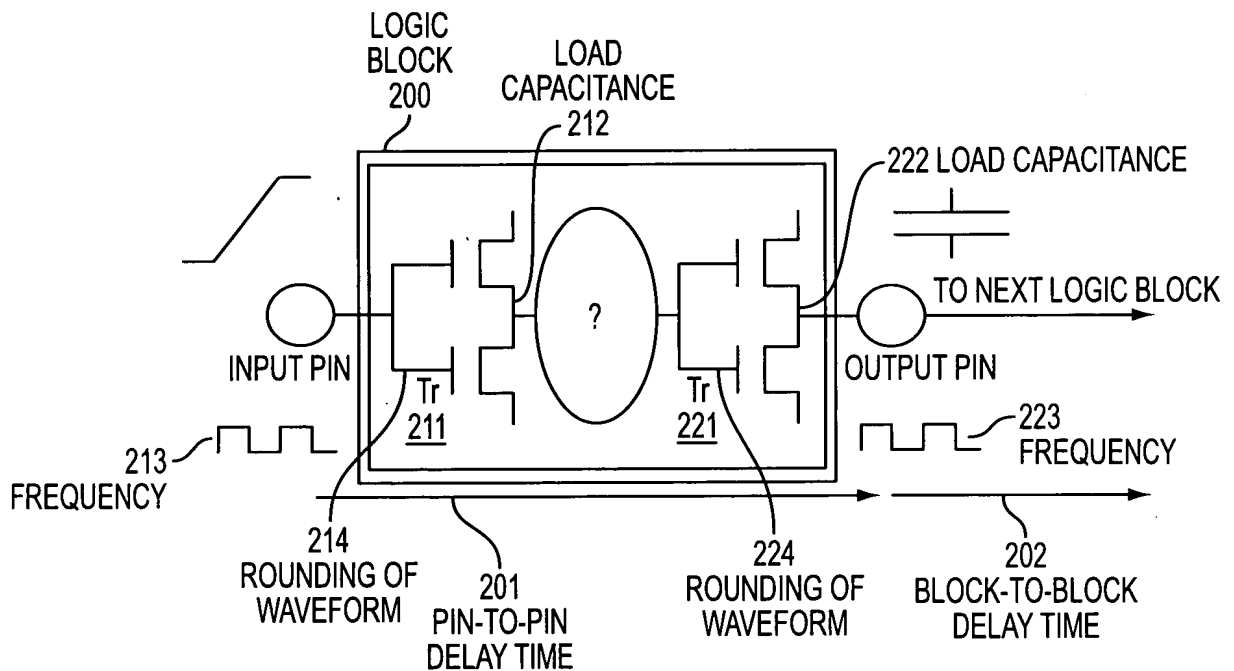
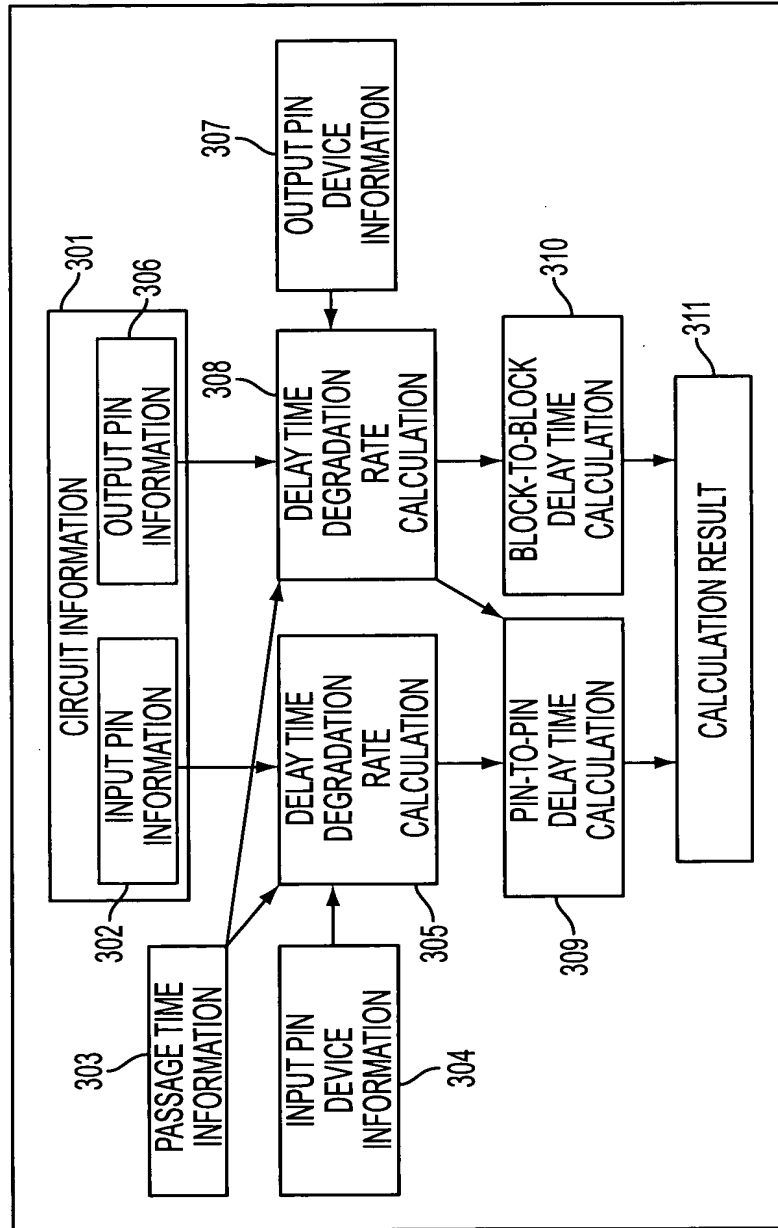


FIG. 2



300 DELAY TIME CALCULATION METHOD

FIG. 3

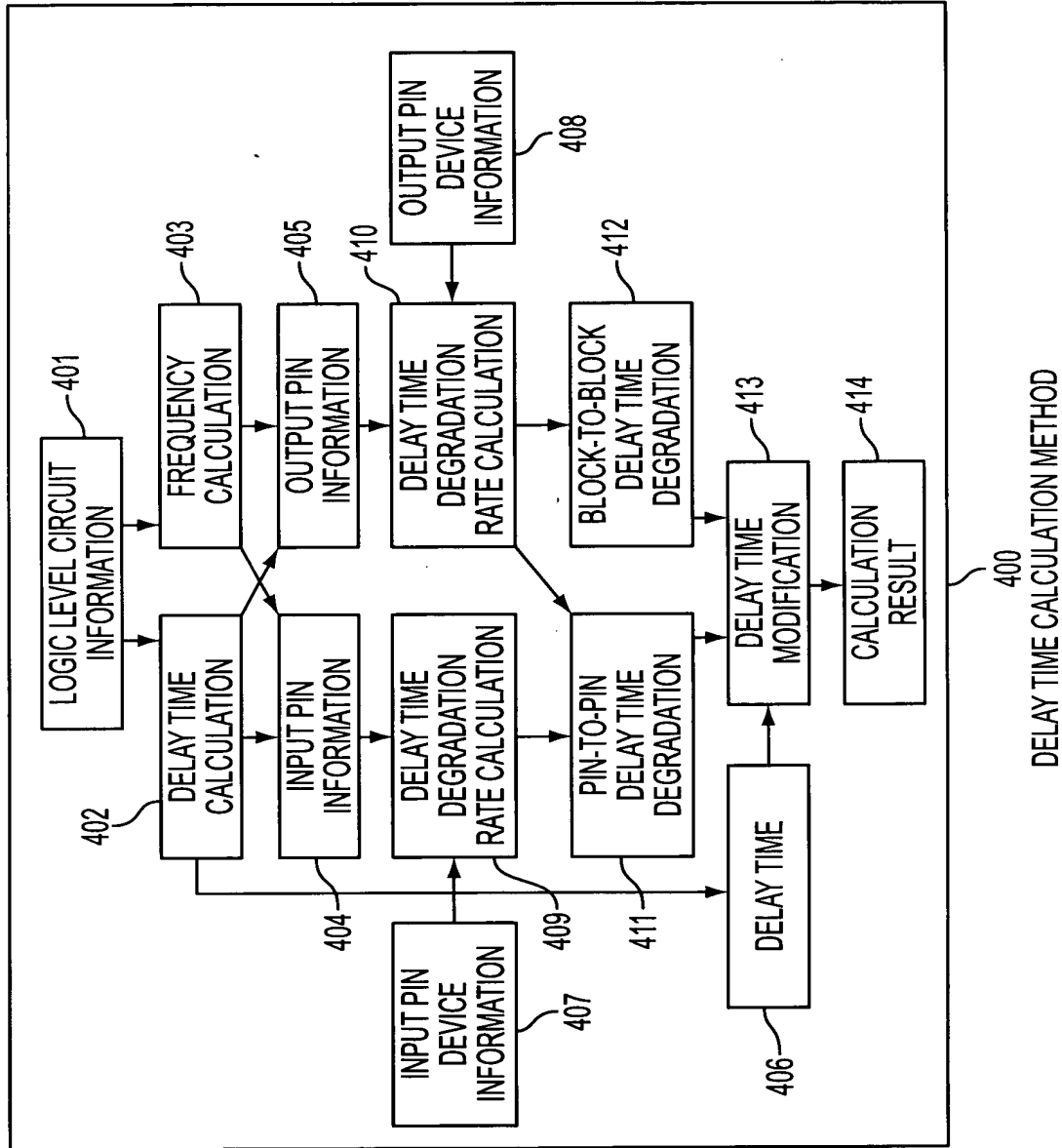


FIG. 4

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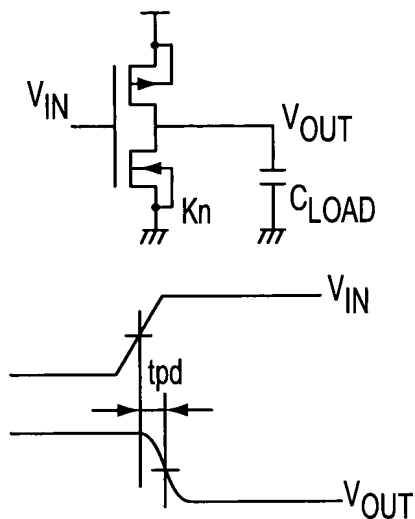


FIG. 5

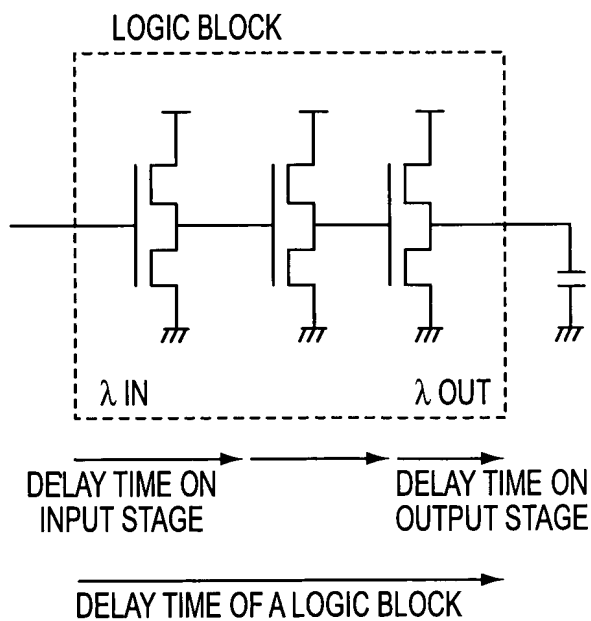


FIG. 6